Linköping University
INSTITUTE OF TECHNOLOGY

Brief overview and examples of research work

Division of Integrated Circuits and Systems

Department of Electrical Engineering

Division of Integrated Circuits and Systems – Brief background

- A constellation of two former well-established research groups, '*Electronic Devices*' and '*Electronics Systems*', merged in 2014.
- About 30 years research experience in integrated circuits and systems design.
- Internationally recognized as one of the forerunners in high-speed, low power CMOS circuits and signal processing techniques (in most course books).
- Several techniques and concepts utilized in commercial products such as advanced microprocessors, wireless sensors, internet routers, CMOS cameras, data acquisition systems, and more.
- Strong tradition of collaboration with industry and academia worldwide.
- Produced about 8 full Professors, and more than 60 PhDs who are currently with European and U.S. companies, such as Ericsson, SAAB, Infineon, Intel, Broadcom, NXP, etc.
- State-of-the-art laboratories and IC design environment.
- Provide broad education including about 20 courses at basic and advance levels within digital, analog, and radio frequency integrated circuits and systems.

Research – Efficient analog, digital, and radio frequency integrated circuits and systems

Mixed Analog/Digital

- Data converters (ADCs and DACs) for high data-rate communications, low-power sensors, and medical implant devices.
- High-precision analog readout and data acquisition for image sensors and other massive parallel sensors .
- Integrated power management systems and power converters for energy harvesting.
- On-chip clock generators, frequency synthesizers, and timing/synchronization.
- High-speed on-chip/off-chip communication links and I/O interface.

Digital

- High-performance and low-power integrated digital processing circuits and systems.
- On-chip networks and on-chip memories.

Radio Frequency (RF) IC

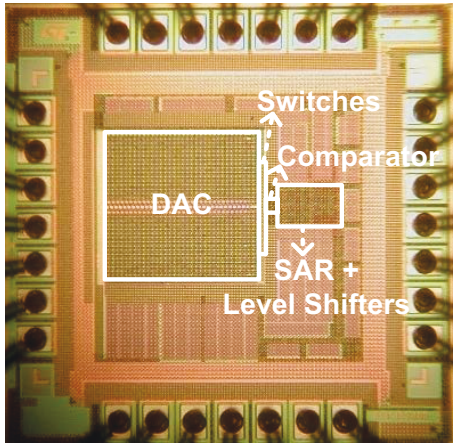
- Energy-efficient RF CMOS power amplifiers and radio transmitter front-ends.
- Flexible RF sampling receiver front-ends for software defined radio.
- Low-power wireless transceivers for wireless sensors..

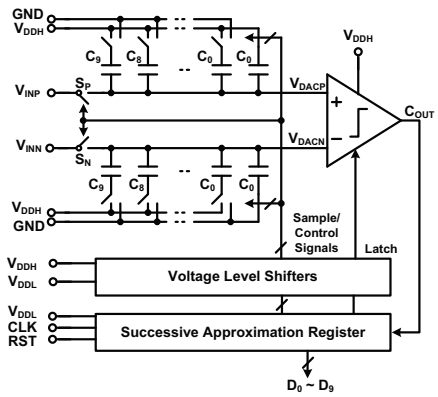
Examples of IC design projects and results

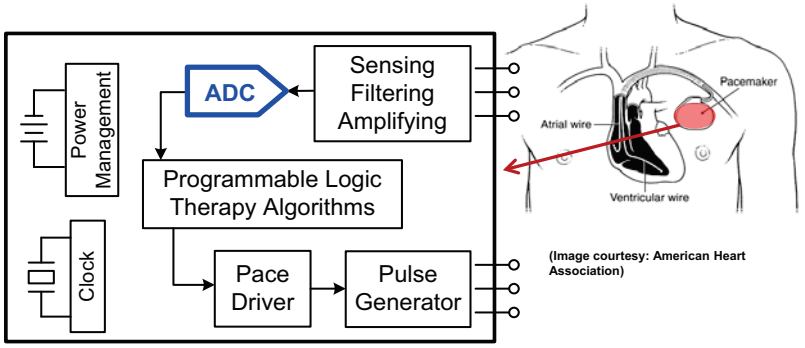
** The material will be updated every year to include new examples of the ongoing projects and our latest published research work.*

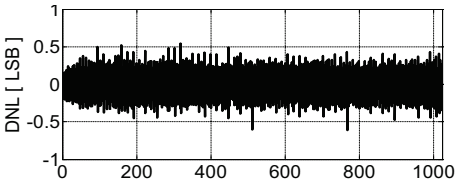
Efficient Data Converters (ADCs and DACs)

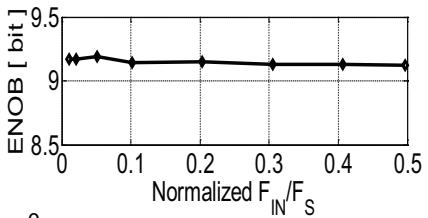
A 53-nW 9.12-ENOB 1-kS/s SAR ADC in 130 nm CMOS for medical implant devices, particularly for pacemakers

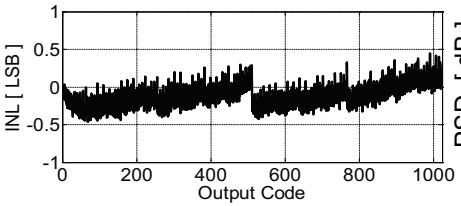


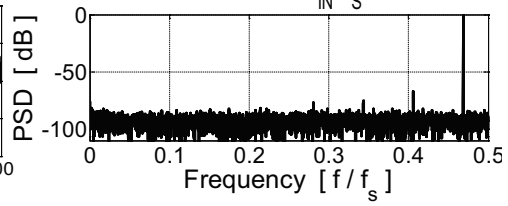










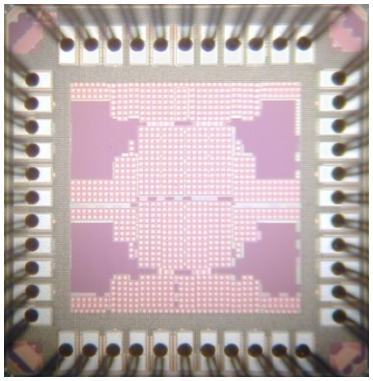


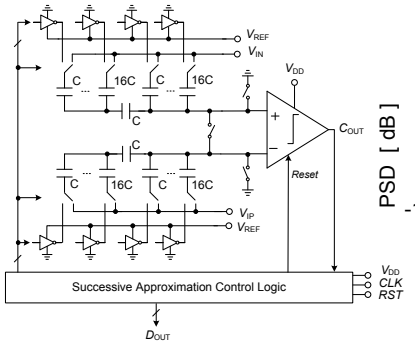
Author/ Year	Sauerbrey 2003 [8]	Bechen 2006 [9]	Zou 2009 [10]	This Work
Technology [µm]	0.18	0.8	0.35	0.13
Sample Rate [kS/s]	4.1	0.8	1	1
Power [nW]	850	3000	230	**53**
ENOB [bit]	6.9	9	10.2	9.1
FoM [fJ/Conv.]	1700	7300	195	**94.5**

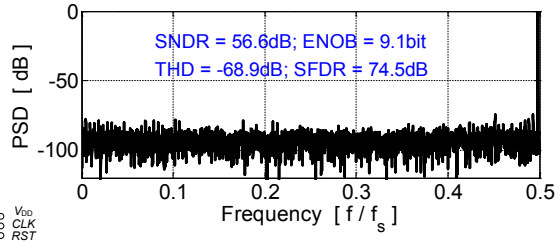
Lowest reported power consumption (53 nW) in 2012 for ADCs for such applications!

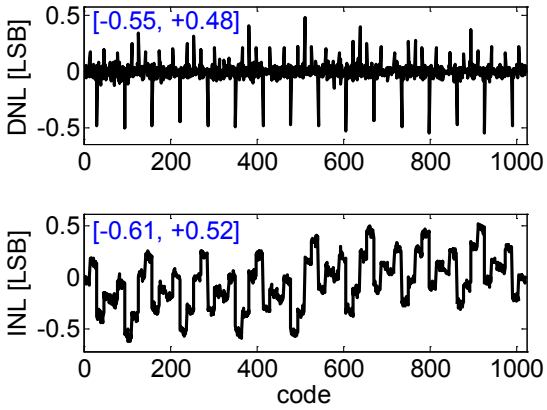
D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-µm CMOS for Medical Implant Devices", in IEEE Journal of Solid-State Circuits, vol.47, no.7, pp.1585-1593, July 2012.

A 3-nW 9.1-ENOB SAR ADC at 0.7 V and 1 kS/s in 65nm CMOS, for medical implant devices and ultra-low-power sensors.









Single supply low-voltage (700mV) and multi-Vt design

ADC Measurement Summary

Technology	65 nm CMOS
Core area [mm^2]	0.037
Resolution [bit]	10
Input range [V]	0 - V_{DD}
Sampling rate [kS/s]	1
Supply voltage [V]	0.7
DNL [LSB]	+0.48/-0.55
INL [LSB]	+0.52/-0.61
SNDR (near Nyquist) [dB]	56.6
SFDR (near Nyquist) [dB]	74.5
THD (near Nyquist) [dB]	-68.9
ENOB [bit]	9.1
Total power [nW]	3
FOM [fJ/Conv.]	5.5

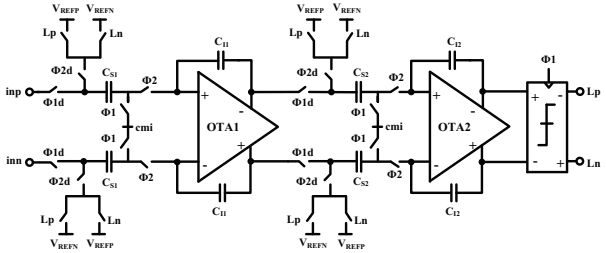
ADC Comparison

	[7]	[8]	[2]	[9]	This Work
Technology	0.35 μm	0.18 μm	0.13 μm	65 nm	65 nm
Sampling rate	1 kS/s	4.1 kS/s	1 kS/s	20 kS/s	1 kS/s
Area [mm^2]	N/A	0.11	0.19	0.212	0.037
Supply voltage [V]	1.0	0.5	1.0/0.4	0.55	0.7
Power [nW]	230	850	53	206	3
ENOB [bit]	10.2	6.9	9.1	8.84	9.1
FOM [fJ/Conv.]	195	1700	94.5	22.3	5.5

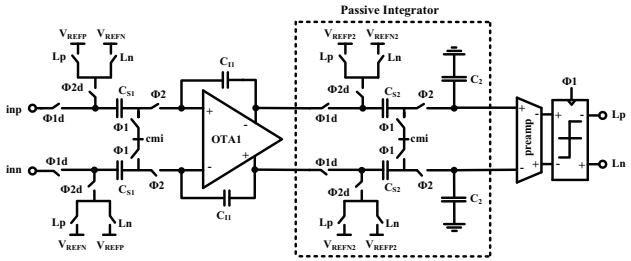
Lowest reported power consumption of 3 nW, pushed the power limits in 2012, as compared to previously lowest reported power, also from us (in previous slide)

D. Zhang, A. Alvandpour, "A 3-nW 9.1-ENOB SAR ADC at 0.7 V and 1 kS/s", in proceedings of the European Solid-State Circuit Conference (ESSCIRC), pp.369-372, Bordeaux, France, September 2012

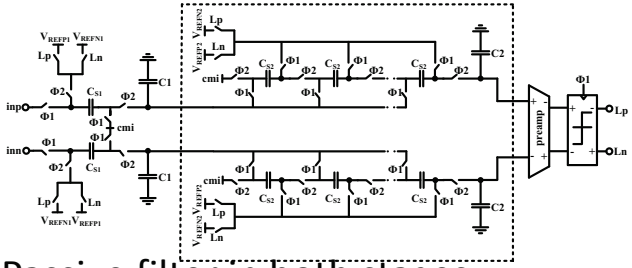
Low-Power ADC DT ΔΣ modulators using SC passive (OTA-less) filters in 65nm CMOS



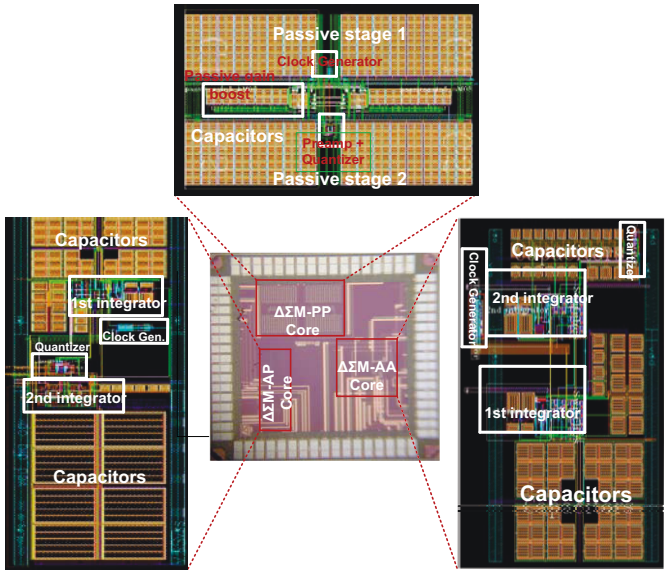
Active filters in both stages ($\Delta\Sigma_{AA}$)



Passive filter in 2nd stage ($\Delta\Sigma_{AP}$)



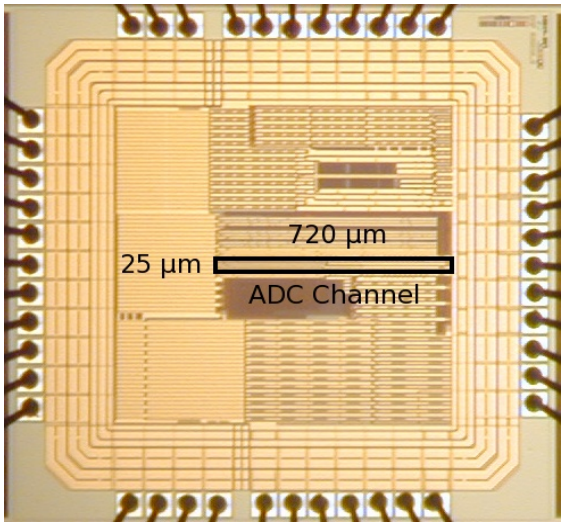
Passive filter in both stages (OTA-less modulator, $\Delta\Sigma_{AP}$)

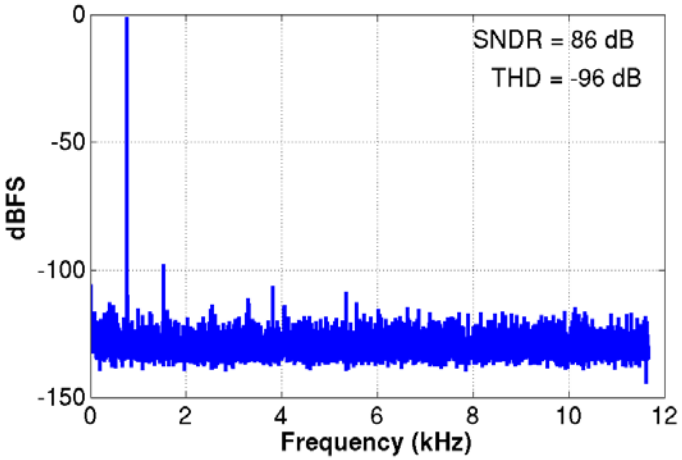


	$\Delta\Sigma M_{AA}$	$\Delta\Sigma M_{AP}$	$\Delta\Sigma M_{PP}$
Technology	1P7M 65nm CMOS		
Supply Voltage	0.9-V		0.9-V / 0.7-V
Clock Frequency	250-kHz		500-kHz
Signal BW	500-Hz		
Peak SNR	80 dB	73.5 dB	70.2 dB / 68 dB
Peak SNDR	76 dB	70 dB	67 dB / 65 dB
Dynamic Range	75 dB	70.5 dB	55 dB / 53 dB
Power	2.1 μW	1.27 μW	0.92 μW /0.43 μW
Active Area mm^2	0.033	0.059	0.125
FOM_W pJ/step	0.407	0.491	0.503 / 0.296

A. Fazli, F. Qazi, and A. Alvandpour, "Low-Power DT ΔΣ Modulators Using SC Passive Filters in 65 nm CMOS," *In IEEE Transaction on Circuits and Systems I*, pp. 358-370, Vol. 61, No. 2, Feb 2014

A compact 16-bit ADC for infrared readout IC



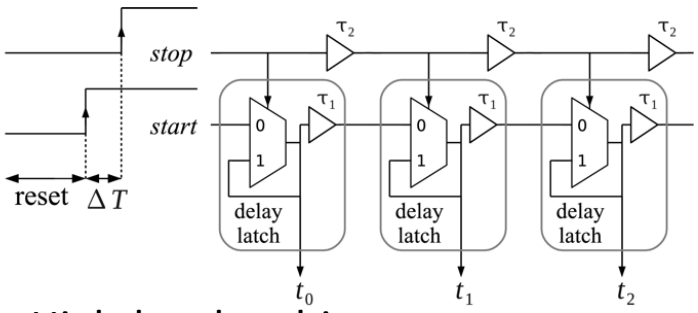


- Utilized in a column-parallel readout structure
- Compact architecture and shared circuitry allows individual channels fit in a 25-µm pitch
- Chopper stabilization reduces offset and 1/f noise

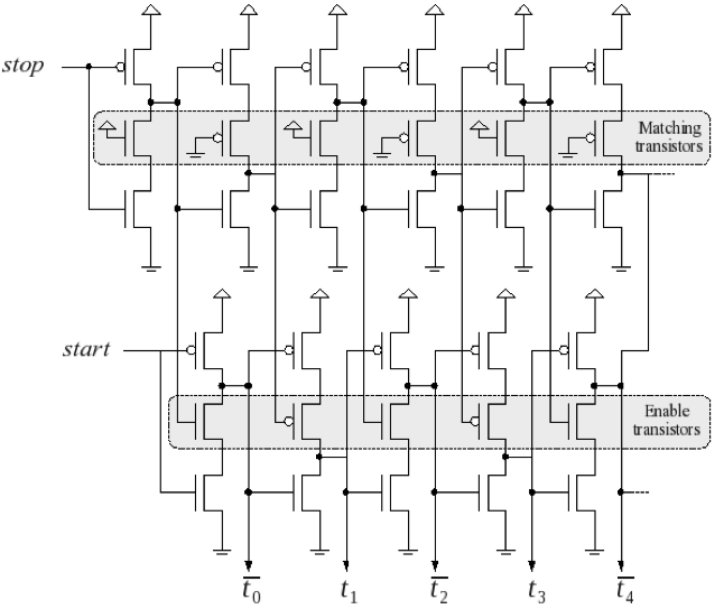
Process	0.35 µm CMOS
Sample Rate	23.32 kHz (60 fps)
SNDR	86 dB
THD	-96 dB
Dynamic Range	90 dB
- ADC Channel power - Common Circuitry	570 µW 24 mW (292 channels)
ADC Channel	0.018 mm^2 (25x720 µm)

D. Svärd, C. Jansson, and A. Alvandpour, "A readout IC for an uncooled microbolometer infrared FPA with on-chip self-heating compensation in 0.35 µm CMOS", in Analog Integrated Circuits and Signal Processing, vol. 77, pp. 29 - 44, October 2013

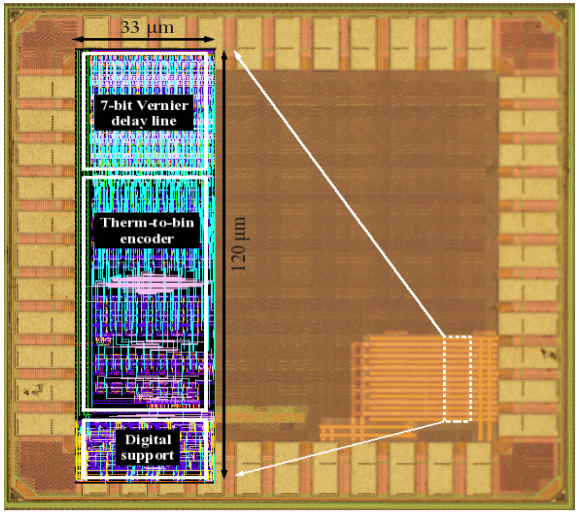
A Vernier time-to-digital converter with delay latch chain architecture



High-level architecture



Detailed implementation



RECENTLY PUBLISHED TDCS

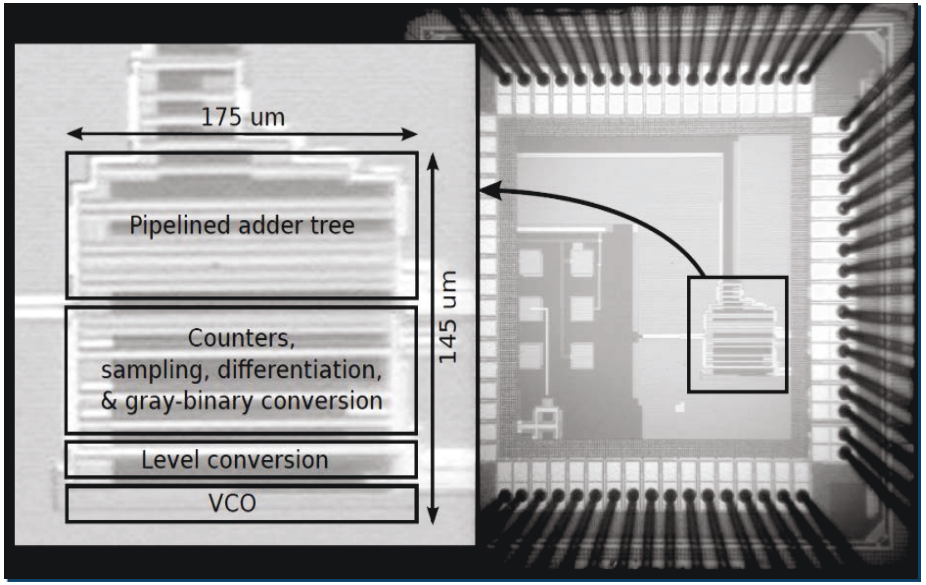
Type	[14] Passive interp.	[15] Cyclic Vernier	[16] 2-D delay line	[17] Vernier + GRO	This Work
Samp. rate [MS/s]	180	10	50	25/100	100
Resolution [ps]		5.5	4.8	5.8	5.7
Oversampling ratio	4			16	
Res. w. interp. [ps]	4.7			3.2	
Power supply [V]	1.2	1.0	1.2	1.2	1.2
Power [mW]	3.6	2.0	1.7[a]	3.6[b]	1.14/1.75[c]
Range [ns]	0.6	100	0.6	40	0.73
Number of bits	7	15	7		7
Area [mm^2]	0.02	0.006	0.02	0.027	0.004
Technology [nm]	90		65	90	65
Year	2008	2011	2010	2012	2013

[a] measured at 50 MS/s
[b] measured at 25 MS/s
[c] measured at 50/100 MS/s

N.U. Andersson and M. Vesterbacka, "A Vernier Time-to-Digital Converter With Delay Latch Chain Architecture," IEEE Trans. Circuits Syst. Part II: Express Briefs, vol. 61, no. 10, pp. 773-777, Oct. 2014.

Synthesizable all-digital ADCs

Example: A time-mode ADC in 65nm CMOS using standard cells



Performance metric	[14]	[17]	[13]	[12]	This work
Sampling (MHz)	300	500	600	640	205
OSR	5	25	15	16	4
Bandwidth (MHz)	30	10	20.0	20.0	25.62
ENOB	8.3	9[a]	8.43[a]	7.35[a]	8.1
SNDR (dB)	52	56[b]	52.5	46	50.3
SNR (dB)	-	63.1	55.1	46.2	52.8
SFDR (dB)	54	72	64.0	67	55.3
Power (mW)	5.7	12.6	14.3	6.3[c]	3.3
FoM (fJ/step)	294	1010	1040[d]	960[d]	235
Area (mm^2)	0.009	0.078	0.12	0.026	0.026
Synthesizable[e]	-	-	-	-	Yes
Technology (nm)	65	130	130	90	65

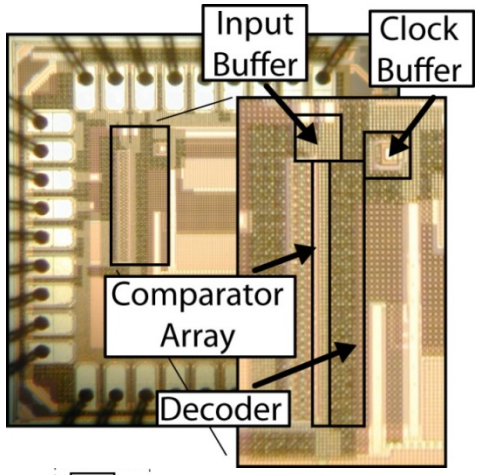
[a] ENOB computed from SNDR, using ENOB = (SNDR − 1.76)/6.02.
[b] Data estimated graphically from the plot presented.
[c] No power overhead due to digital correction.
[d] FoM computed using FoM = $P_{avg}/(2^{ENOB}2B)$.
[e] Components from a standard digital cell library.

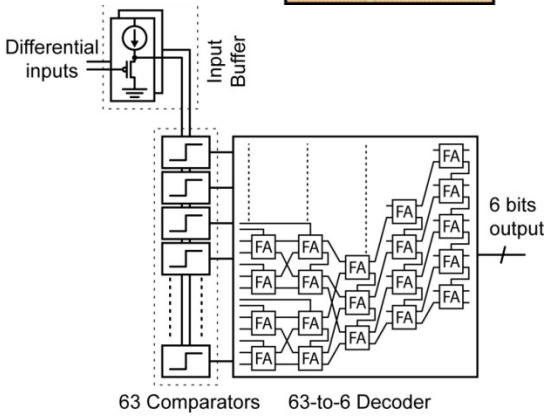
- Signal represented and processed in time instead of voltage/current.
- Ring VCO based noise-shaping, all-digital
- Exclusive use of vendor supplied standard cells
- Spurious-error mitigation using Gray-counter based phase accumulation
- Lowest reported power consumption and best FoM in class

V. Unnikrishnan and M. Vesterbacka, "Time-mode analog-to-digital conversion using standard cells," in IEEE Transactions on Circuits and Systems I, Volume 61, Issue 12, pp. 3348 - 3357, December 2014

Energy-efficient high-speed Flash ADCs

Example: A low-power 4-bit, 1.5 to 2.5 GHz Flash ADC in 90nm CMOS





- Redundancy-based flash ADC, 63 small-sized comparators for 4-6 bits of resolution.
- Calibration by disabling bad comparators
- The ADC utilizes native mismatches (process variations) and redundancy to generate the references voltages without using reference ladder.

Author Year	ENOB	Sampling Freq.	CMOS Process	Power	FoM pJ/Conv-Step
Park. 2007	3.9	4 GS/s	0.18µm	608 mW	20.4
Park, 2005	5.5	2 GS/s	0.18µm	145 mW	6.41
Sheikhaei, 2007	3.2	3.0 GS/s	0.18µm	43 mW	1.51
Deguchi, 2007	4.9	3.5 GS/s	90nm	98 mW	0.95
Lin, 2007	4.2	4.2 GS/s	0.13µm	180 mW	2.80
Van der Plas, 2007	3.7	1.25 GS/s	90 nm	2.5 mW	0.15
Proposed Flash ADC	**3.9**	**2.5 GS/s**	**90nm**	**30 mW**	**3.15**
Proposed reference-free Flash ADC	**3.7**	**1.5 GS/s**	**90nm**	**23 mW**	**1.47**

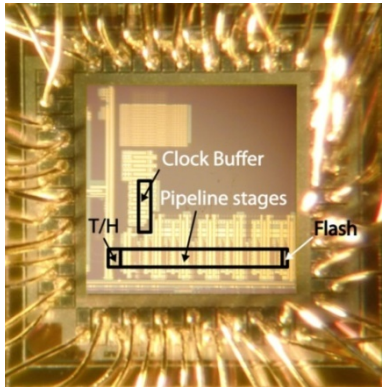
T. Sundström and A. Alvandpour, "Utilizing Process Variations for Reference Generation in a Flash ADC", in IEEE Trans. Circuits and Systems II, Vol 56, Issue 5, pp. 364 - 368, May 2009.

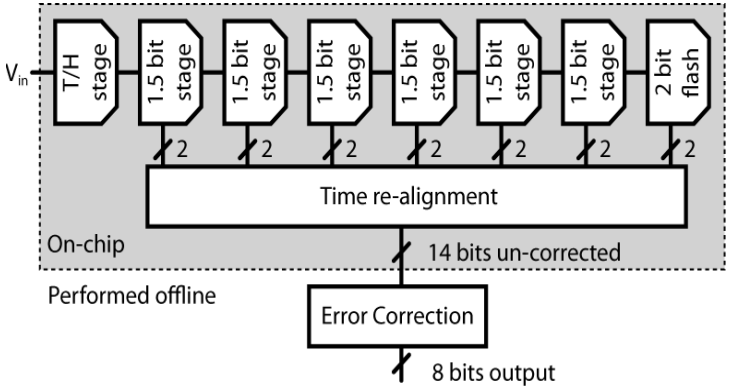
T. Sundström and A. Alvandpour, "A 6-bit 2.5-GS/s Flash ADC using Comparator Redundancy for Low Power in 90nm CMOS," in Analog Integrated Circuits and Signal Processing, Vol.64, pp. 215-222, Aug 2010.

High-speed pipeline ADCs for wideband communications

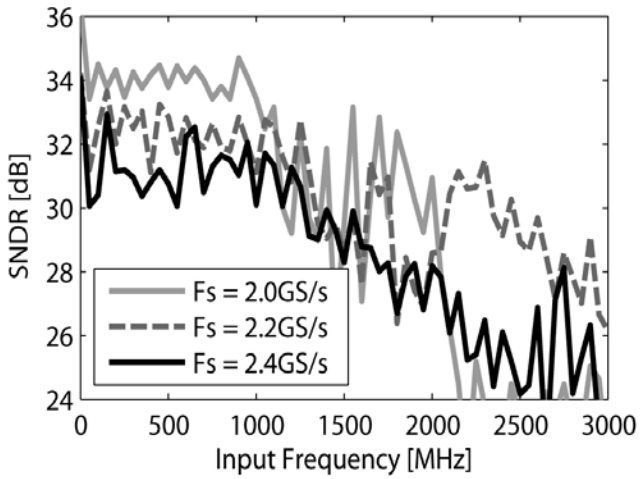
Example:

A 2.4 GS/s, Single-Channel, 31.3 dB SNDR at Nyquist, 8-bit Pipeline ADC in 65nm CMOS





- Clocking scheme removes the comparator latency from the critical path.
- Fast open-loop amplifiers
- Digital calibration, corrects for stage gain-error and input-stage non-linearity.

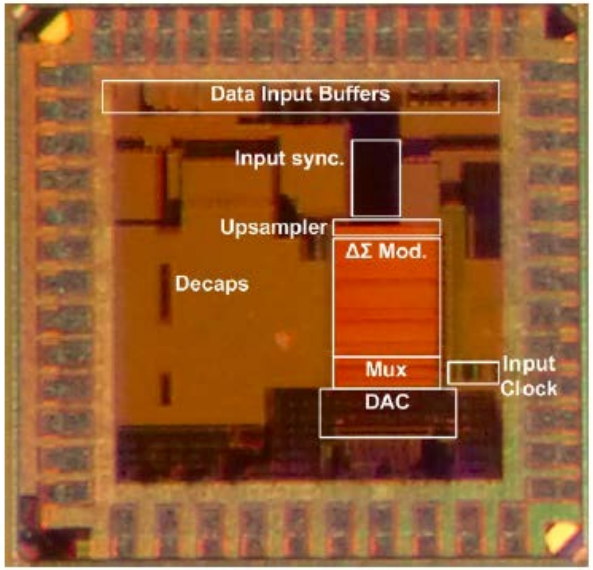


Author Year	Architecture	CMOS Process	Sample Rate (GS/s)	$ENOB_{min}$ DC-Nyquist	Power (mW)	FoM (pJ/conv-step)
Shen JSSC-07	Pipeline	0.18µm	0.8	4.9	105	3.3
Varzaghani JSSC-09	Interleaved Pipeline	0.13µm	4.8	4.7	300	2.3
Nazemi VLSI-08	Interleaved Pipeline	90nm	10.3	5.1	1600	2.8
This Work	**Pipeline**	**65nm**	**2.0** **2.2** **2.4**	**5.3** **4.9** **4.7**	**294** **310** **318**	**2.7** **3.4** **3.2**

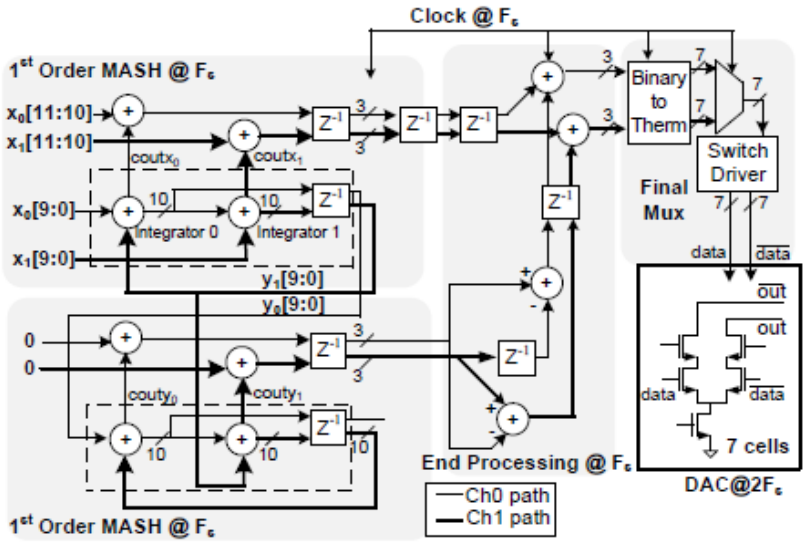
Fastest reported CMOS pipeline ADC in 2011

T. Sundström, C. Svensson, A. Alvandpour, "A 2.4 GS/s, Single-Channel, 31.3 dB SNDR at Nyquist, 8-bit Pipeline ADC in 65nm CMOS," in IEEE Journal of Solid State Circuits, vol. 46, pp. 1575-1584, July 2011

An 8-GS/s 200-MHz bandwidth 68-mW ΔΣ DAC in 65-nm CMOS for wideband radio transmitters

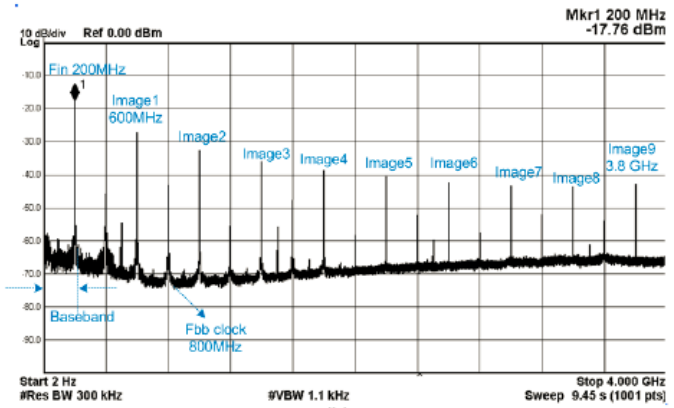


Two-channel interleaved



8GS/s at 200 MHz BW
57dB IM3, 48dB SFDR, 26dB SNDR.
68mW power consumption.

1.5X higher sampling rate and 2X higher bandwidth, compared to previously reported ΔΣ DACs.



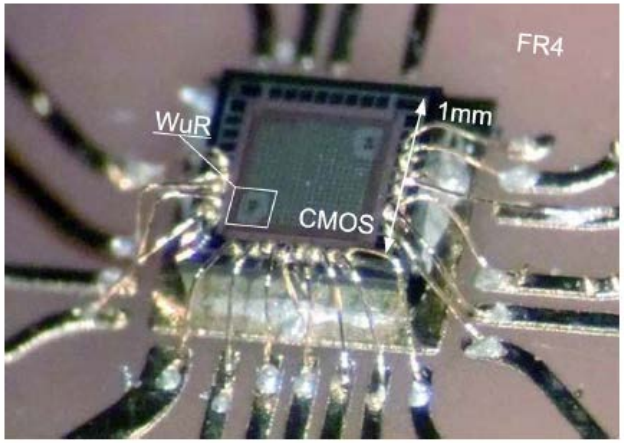
(b)

8GS/s @ 200MHz BW

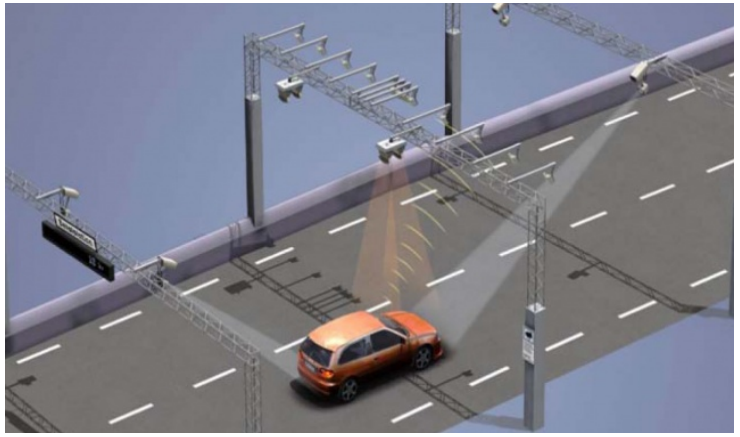
A. Bhide, O. E. Najari, B. Mesgarzadeh, and A. Alvandpour, "An 8-GS/s 200-MHz Bandwidth 68-mW ΔΣ DAC in 65-nm CMOS", in IEEE. Transactions on Circuits and Systems II, vol. 60, pp. 387-391, July 2013.

Wireless sensors

Low power wake-up radio using envelope detector



Ultra Low Power Wake-Up Radio using Envelope Detector and T-Line Voltage Transformer

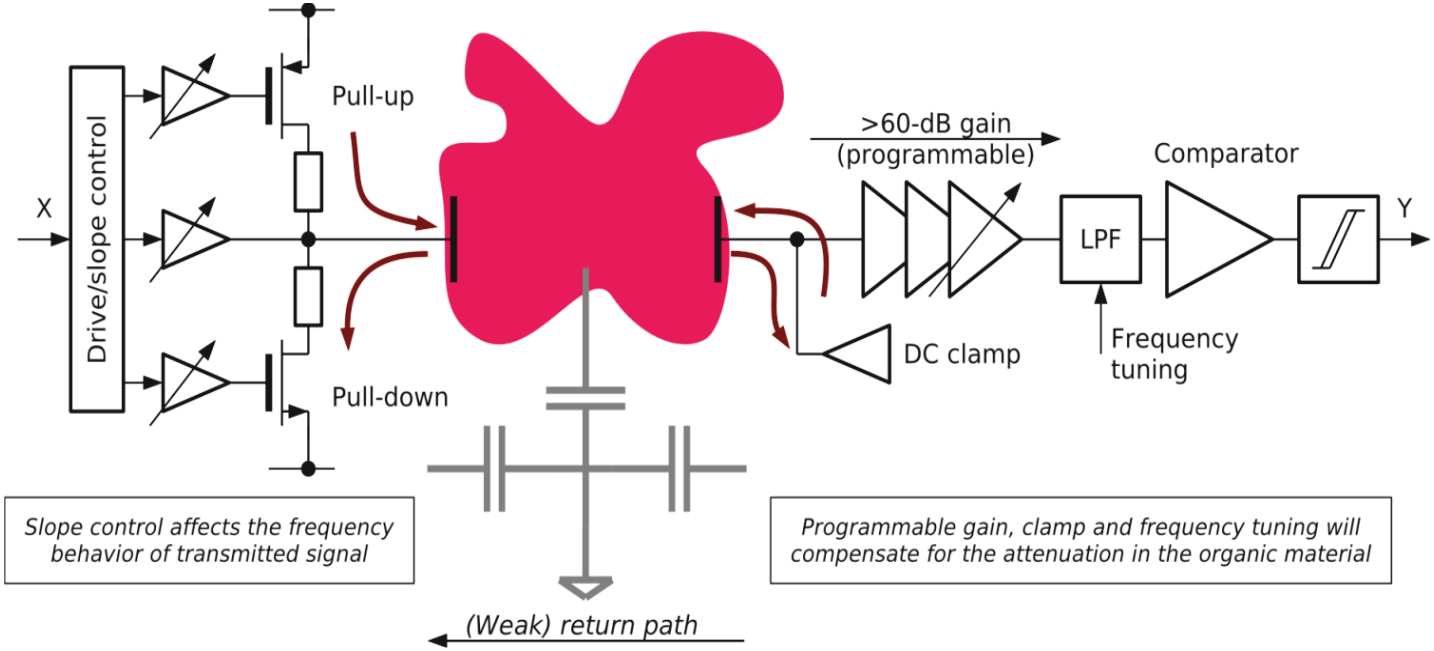


Utilized in an industrial application for automatic toll collection.

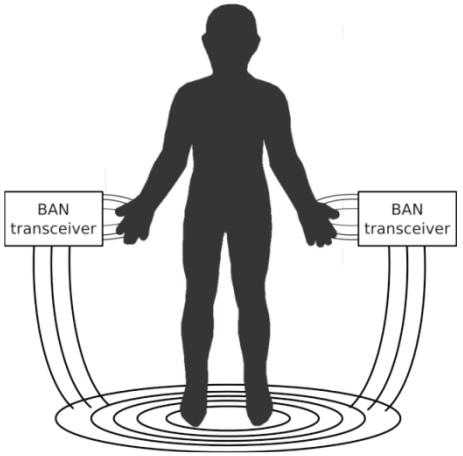
Technology	CMOS 180nm	BAW match, CMOS 90nm	BAW match, CMOS 90nm	Off-chip ind., CMOS 90nm	Schottky, μCtrl	Schottky, μCtrl	CMOS 180nm	FR4 match, CMOS 130nm
Frequency [MHz]	2400	1900	2000	2400	868	860	2400	2450
nJ/bit	0.86	1.6	0.52	0.51	1350	-	0.55	0.023
Bit rate [kbps]	250	40	100	100	0.75	9.6	1.95	200
Sensitivity [dBm]	-86	-50	-72	-64	4.37	-35	-29.8	-47
Power [μW]	215	65	52	51	12.5	10.8	1.08	2.3

E. Nilsson and C. Svensson, "Ultra Low Power Wake-Up Radio using Envelope Detector and Transmission Line Voltage Transformer", in IEEE Journal on Emerging and Selected Topics in Circuits and Systems Volume 3, Issue 1, pp. 5-12 , March 2013.

Analog receiver front-end for body-coupled communication



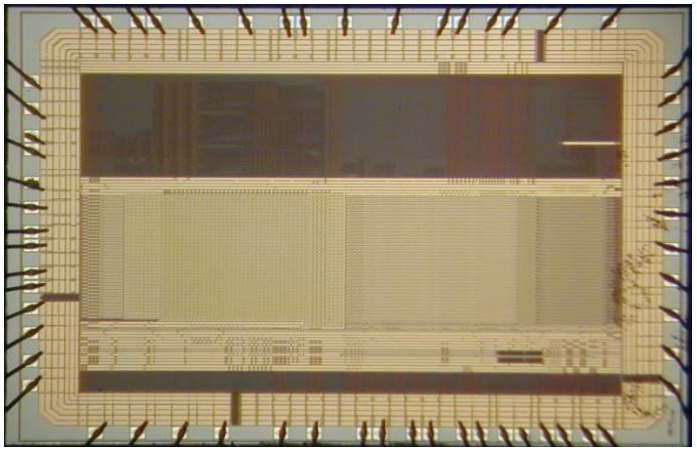
- Power consumption of full AFE < 10 mW
- Integrated in printed electronics labels (Tx) and mobile phones (Rx)
- ID exchange and handshaking

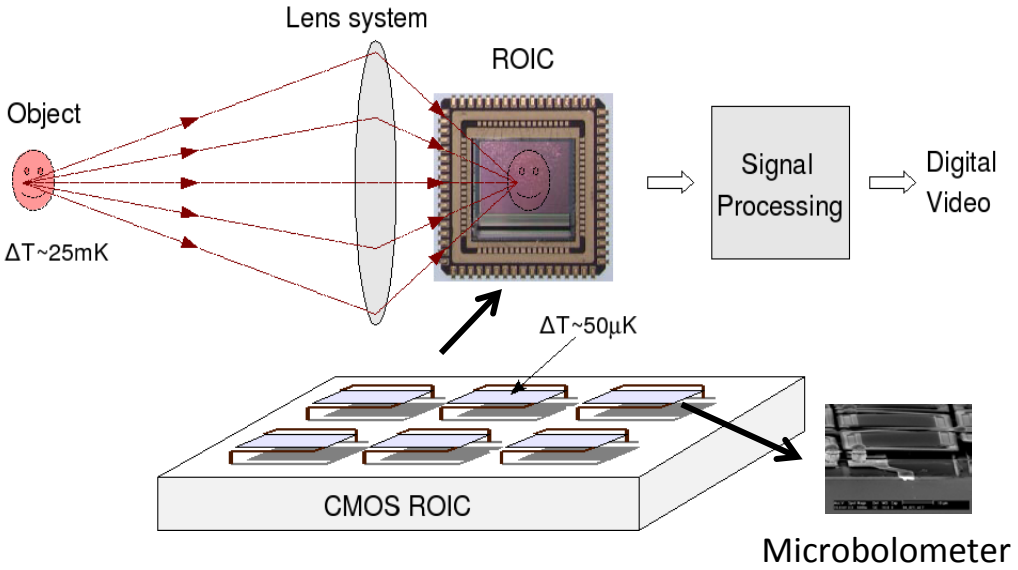


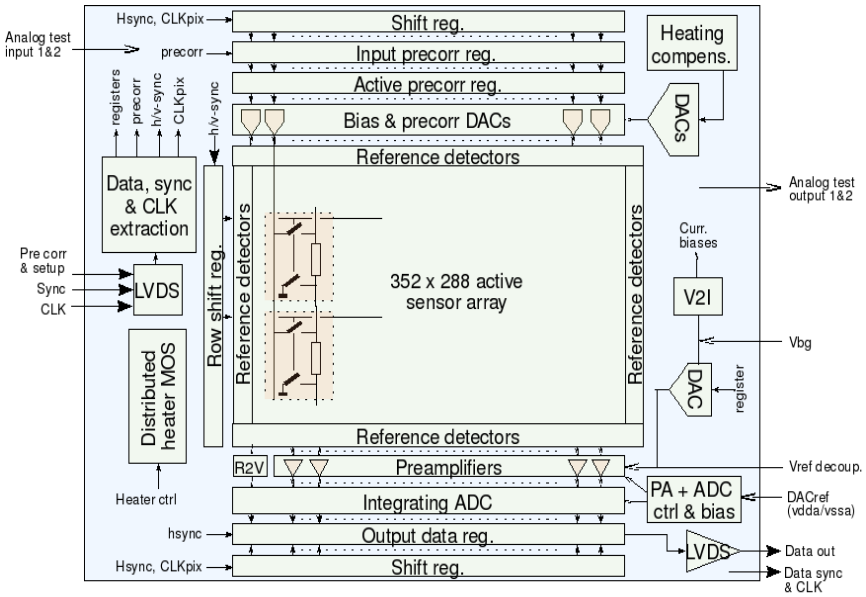
I. Kazim, JJ Wikner, "An analog receiver front-end for capacitive body-coupled communication", in IEEE NorChip 2012, pp 1-4

Integrated sensor readout and data acquisition ICs

Readout IC for an uncooled FPA infrared network camera





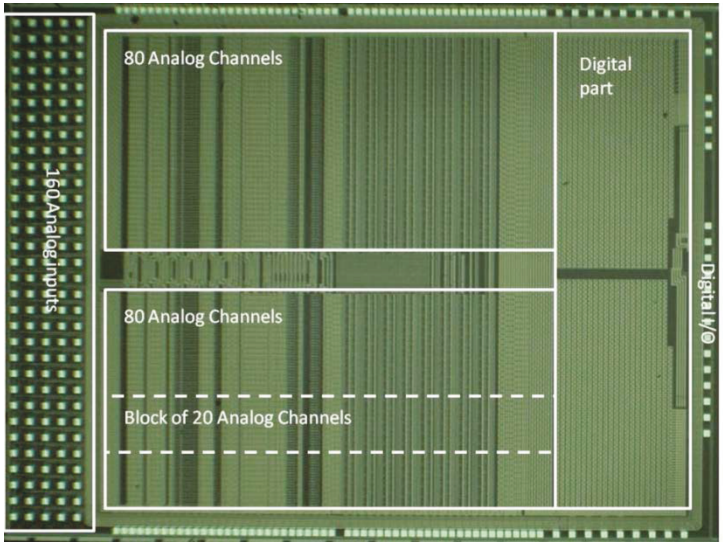


- 288 X 288 Infrared sensor array.
- Column parallel readout with 288 15-bit compact ADCs in 25-µm pitch!

D. Svärd, C. Jansson, and A. Alvandpour, "A readout IC for an uncooled microbolometer infrared FPA with on-chip self-heating compensation in 0.35 µm CMOS", in Analog Integrated Circuits and Signal Processing, vol. 77, pp. 29 - 44, October 2013

A high-rate energy-resolving photon-counting ASIC for spectral computed tomography

In cooperation with Royal Institute of Technology, Stockholm



	Target/Simulation	Measured
Number of channels	160	
Gain	2.08mV/keV	2.10mV/keV
Noise level, ENC	300 electrons @5pF	207 electrons @~4pF,40ns
Number of energy bins	8	
Energy bin counter resolution	8b	
Peak times	10ns, 20ns, 40ns	10ns, 20ns, **40ns**
Maximum count rate	17Mcps @100MHz clock	17Mcps @100MHz clock
Maximum frame rate	38kframes/s @100MHz clock	
Clock frequency	100MHz, 200MHz	100MHz
Power consumption	800mW @ 200MHz clock	670mW @ 100MHz clock
Chip area	5mm x 6.6mm	

Process: 180nm CMOS
1.6 Million transistors

C. Svensson, F. Amin, A. Ehliar, M Gustavsson, A. Björklid, C Xu , "A high-rate energy-resolving photon-counting ASIC for Spectral Computed Tomography", In IEEE Transaction on Nuclear Science, pp. 30-39, February 2012; and in IEEE Transaction on Nuclear Science, pp. 437-445, February 2013.

Efficient radio transceiver front-ends

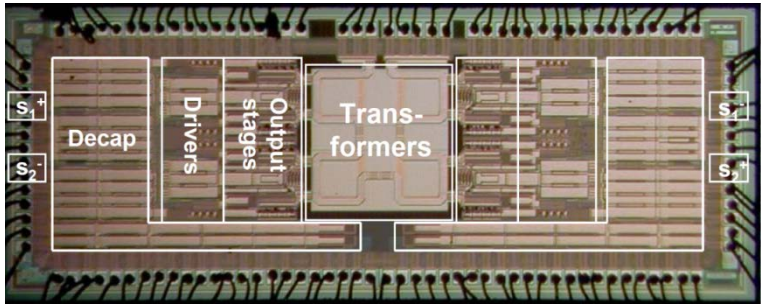
Innovative wideband Class-D outphsing radio power amplifiers

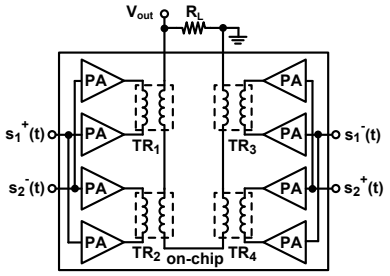
Example 1:

A +32dBm 1.85GHz Class-D Outphasing RF PA in 130nm CMOS for WCDMA/LTE

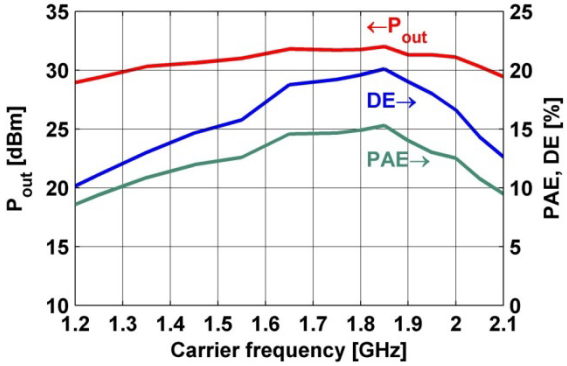
RF Performance

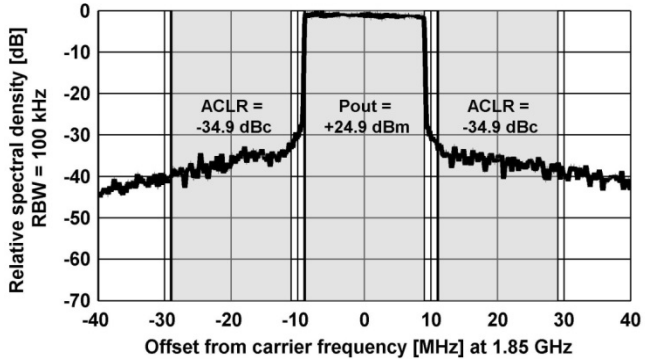
- Pout = +32dBm,
- DE = 20.1%, PAE = 15.3%
- 3dB bandwidth: 0.9 GHz (1.2-2.1 GHz)
- WCDMA (5 MHz)
- PAPR = 3.5dB
- Channel Power: +28dBm
- LTE (20 MHz, 16-QAM)
- PAPR = 6.6dB
- Channel power: +24.9dBm
- No predistortion used





8 Class-D stages, 4 on-chip transformers





Highest reported output power (32 dBm) for CMOS outphasing PAs in 2011!

J. Fritzin, C. Svensson, and A. Alvandpour, "A +32dBm 1.85GHz Class-D Outphasing RF PA in 130nm CMOS for WCDMA/LTE," in IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 127-130, Sept. 2011

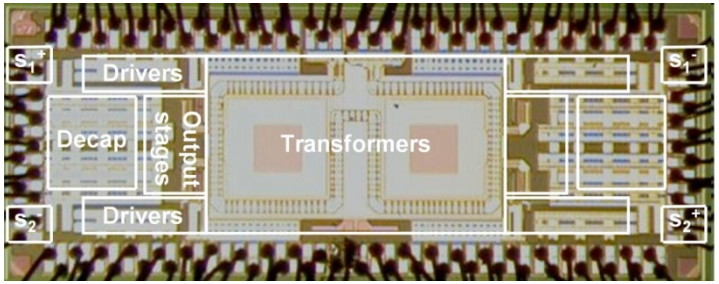
Innovative wideband Class-D outphsing radio power amplifiers

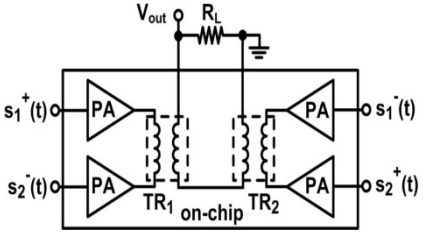
Example 2:

A Wideband Fully Integrated +30dBm Class-D Outphasing RF PA in 65nm CMOS

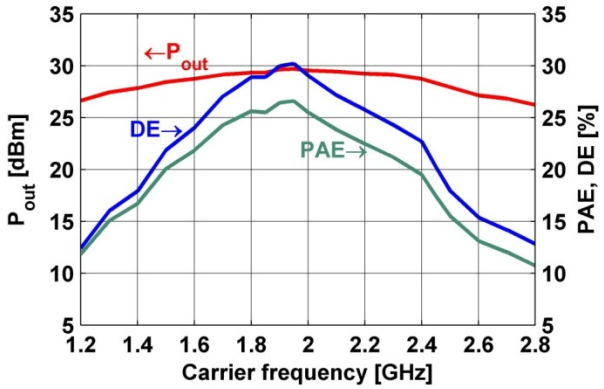
RF Performance:

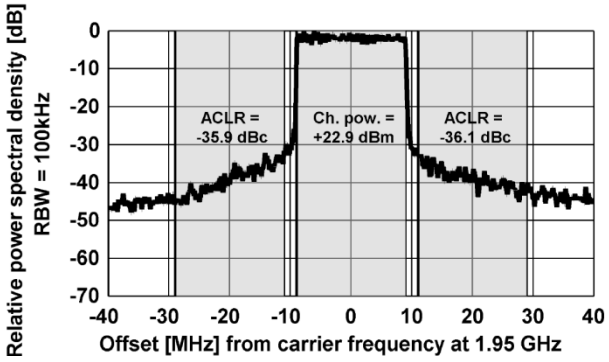
- Pout = +29.7dBm
- DE = 30.2%, PAE = 26.6%
- 3dB bandwidth: 1.6GHz (1.2-2.8GHz)
- WCDMA @ 5 MHz
- PAPR = 3.5dB
- Channel Power: +26dBm
- LTE (20 MHz, 16-QAM)
- PAPR = 6.6dB
- Channel power: +22.9dBm
- No predistortion was used





8 Class-D stages, 4 on-chip transformers



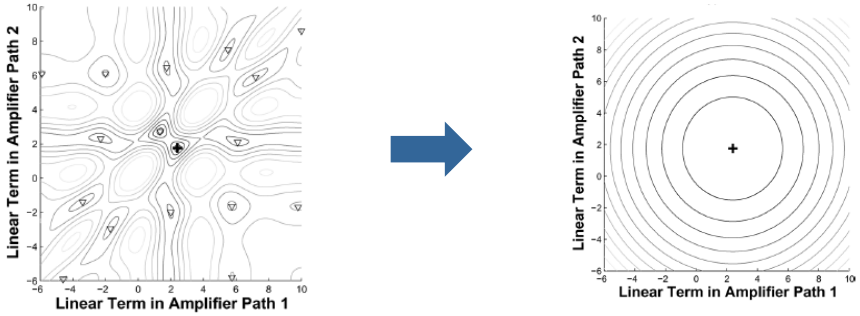


Among highest reported bandwidth (1.6 GHz) for CMOS outphasing PAs

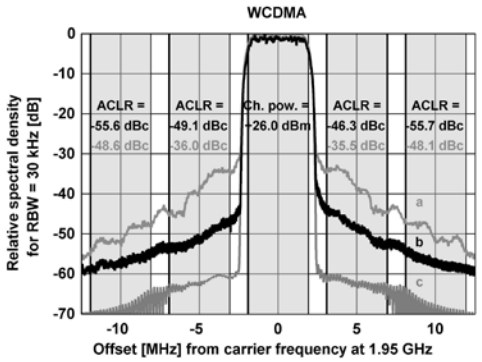
J. Fritzin, C. Svensson, and A. Alvandpour, "Analysis of a 5.5V Class-D Stage Used in +30 dBm Outphasing RF PAs in 130nm and 65nm CMOS," in IEEE Transactions on Circuits and Systems-II, vol. 59, no. 11, pp. 726-730, Nov. 2012.

Innovative predistortion methods for Class-D outphasing PAs, supporting high linearity requirements for radio base-stations

Example:
Least-squares phase predistortion of Class-D outphasing PA in 65nm

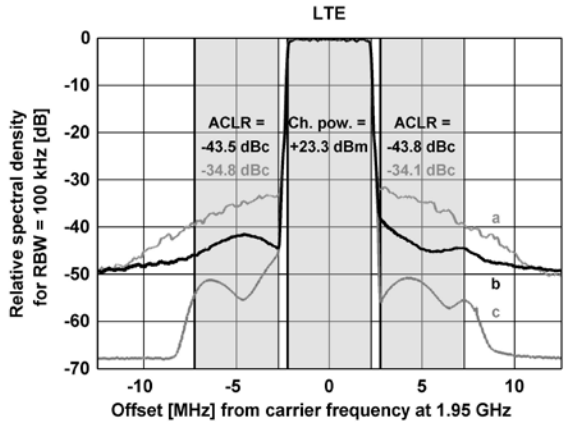


Improved predistortion model from nonconvex to a convex least-squares problem. Predistorter can be calculated analytically.



MEASURED SPECTRAL PERFORMANCE AT 1.95 GHZ FOR WCDMA AND LTE UPLINK SIGNALS WITH PREDISTORTION (USING $n = 5$) AND WITHOUT

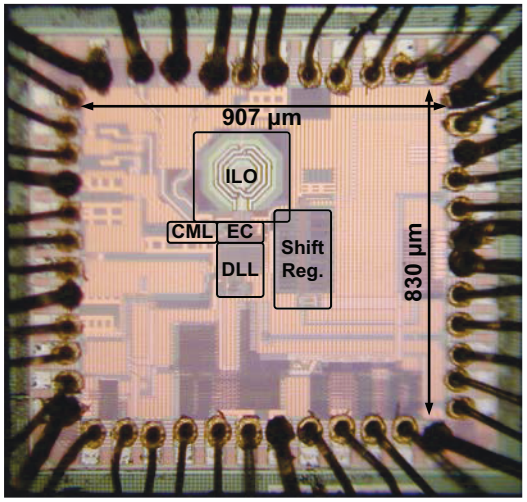
Standard	Measured Parameter	W DPD	W/o DPD	Req
WCDMA	ACLR @ 5 MHz [dBc]	-46.3	-35.5	-33
	ACLR @ 10 MHz [dBc]	-55.6	-48.1	-43
LTE	ACLR @ 5 MHz [dBc]	-43.5	-34.1	-30



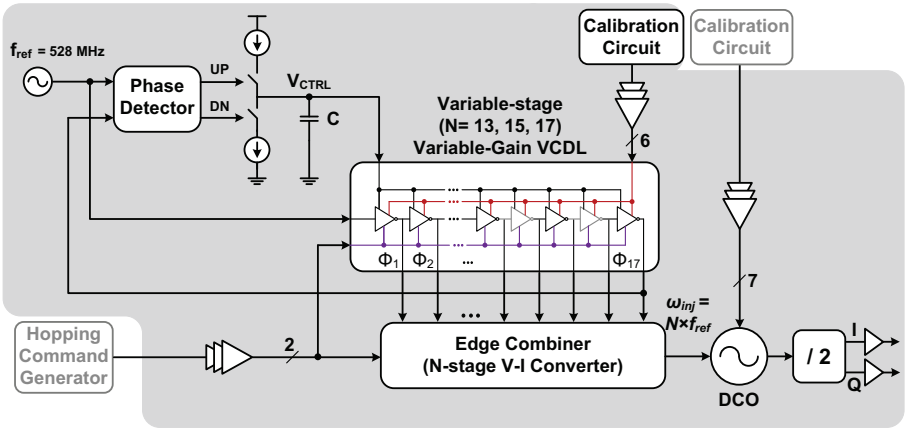
Y. Jung, J. Fritzin, M. Enqvist, and A. Alvandpour, "Least-Squares Phase Predistortion of a +30 dBm Class-D Outphasing RF PA in 65 nm CMOS " in IEEE Transactions on Circuits and Systems I: Regular papers, pp. 1915-1928, vol. 60, nr. 7, July 2013

(a) Measured spectrum without DPD
(b) when DPD is applied to (a)
(c) Spectrum of estimation signal

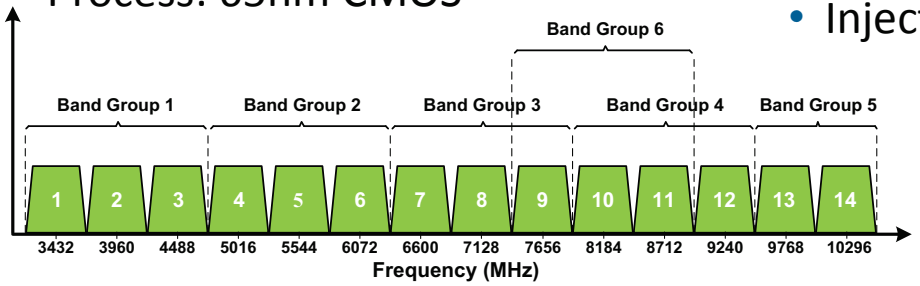
Low-power fast-hopping DLL-based WiMedia UWB synthesizer



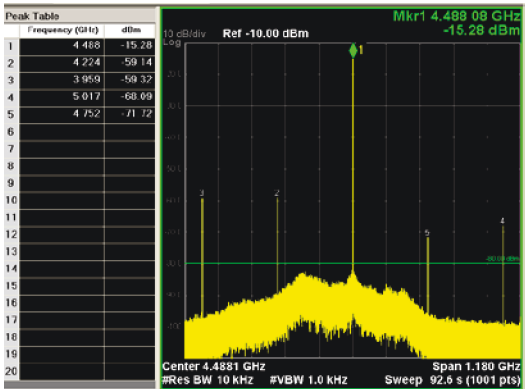
Process: 65nm CMOS



- Open-loop VCDL delay compensation
- PVT calibration
- Injection locked edge combiner

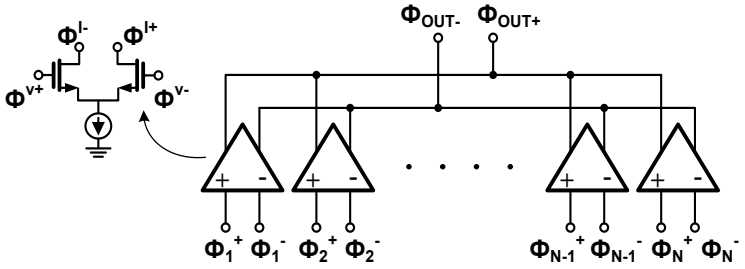


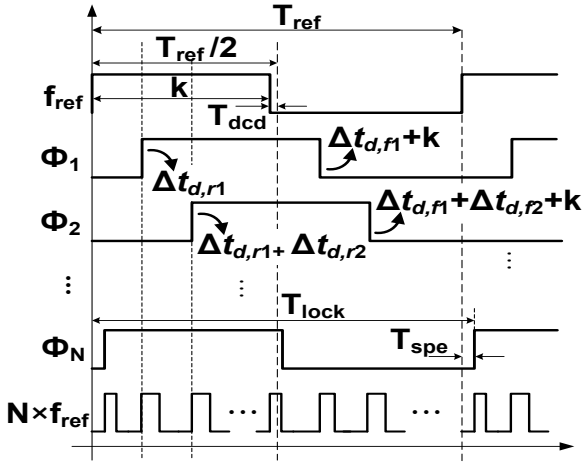
Supports band group 1, with -44dBc spur with power consumption of 21mW



Main concept described in: A. Ojani, B. Mesgarzadeh, and A. Alvandpour, " A DLL-Based Injection-Locked Frequency Synthesizer for WiMedia UWB," in IEEE International Symposium on Circuits and Systems (ISCAS), May 2012, pp. 2027–2030

Efficient modeling and analysis of harmonic spurs in DLL-based frequency synthesizers





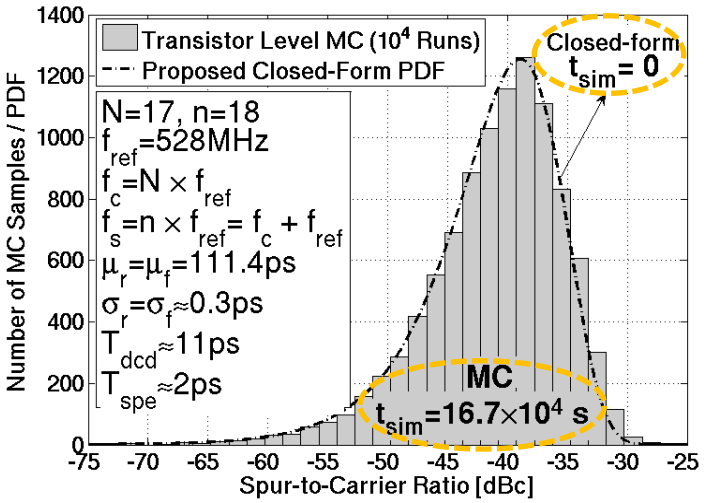
$$p_Z(z)=\begin{cases}\dfrac{z}{\sigma_{cof}^2}\exp\left(-\dfrac{z^2+h^2}{2\sigma_{cof}^2}\right)I_0\left(\dfrac{hz}{\sigma_{cof}^2}\right) & z\geq 0\\ 0 & z<0\end{cases}$$

Probability Density Function (PDF)

$$E[SCR_n]=\sigma_{cof}\sqrt{\frac{\pi}{2}}\exp\left(-\frac{K}{2}\right)\left[(1+K)I_0\left(\frac{K}{2}\right)+KI_1\left(\frac{K}{2}\right)\right]$$

Mean Value

$$h=\sqrt{\mu_{a_n}^2+\mu_{b_n}^2}\qquad \sigma_{cof}\approx\sigma_{a_n}\approx\sigma_{b_n}\qquad K=\frac{h^2}{2\sigma_{cof}^2}$$



Proposed analytical expressions simplify the design process of DLL-based frequency synthesizers by removing the need for exhaustive Monte-Carlo simulations!

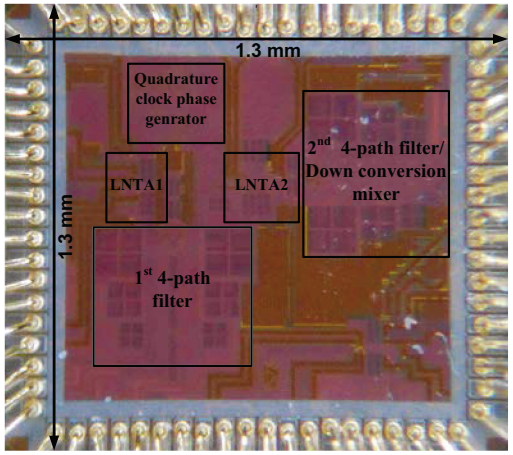
A. Ojani, B. Mesgarzadeh, and A. Alvandpour, "Modeling and Analysis of Harmonic Spurs in DLL-Based Frequency Synthesizers," in IEEE Transactions on Circuits and Systems I, pp. 1–10, Jun. 2014.

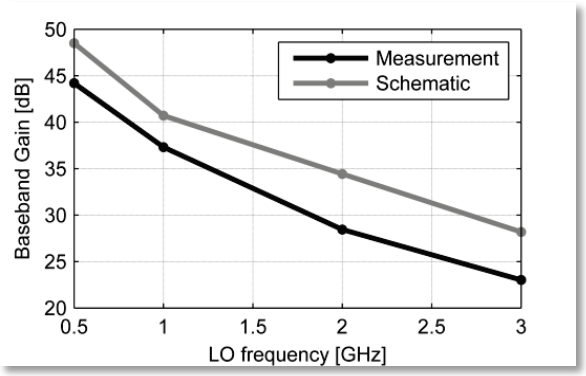
A. Ojani, B. Mesgarzadeh, and A. Alvandpour "Monte Carlo-Free Prediction of Spurious Performance for ECDLL-Based Synthesizers," in IEEE Transactions on Circuits and Systems I, accepted, Aug. 2014.

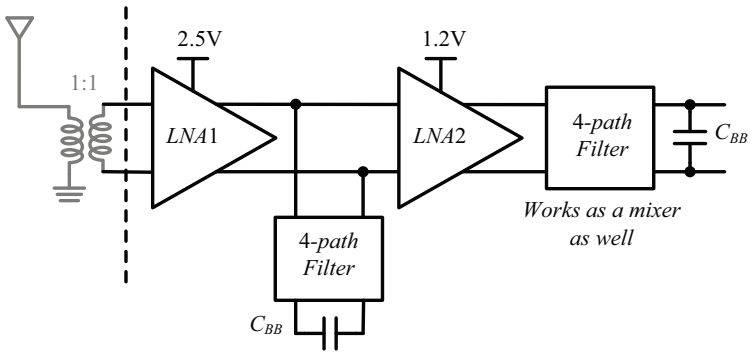
Radio receiver frontends with high blocker rejection capability

Example:

A two-stage highly selective receiver front-end based on impedance transformation filtering.





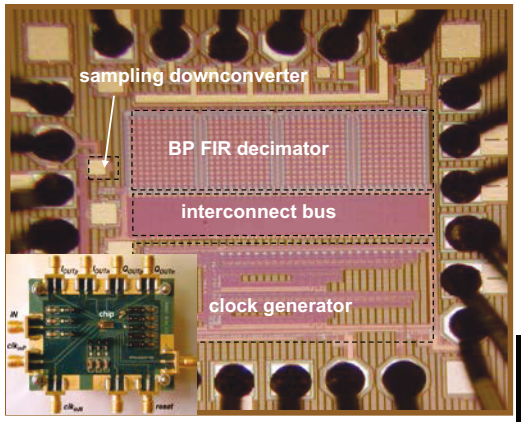


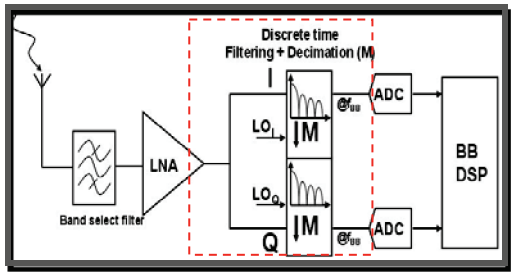
Front-end Architecture	Zero-IF
Technology	65 nm
System	Front-end
Frequency [GHz]	0.5 – 3
Gain [dB]	45 – 25
NF [dB]	3.2 – 5.3
NF@0dBm blocker [dB]	12@100 MHz offset for 2 GHz LO
Blocker Rejection	**60- 38 dB**
Out-of-band IIP3@100MHz [dBm]	+20
Blocker P_{1dB}@100MHz [dBm]	+5
Power Consumption [mW]	46 – 113
Chip area [mm^2]	1.7

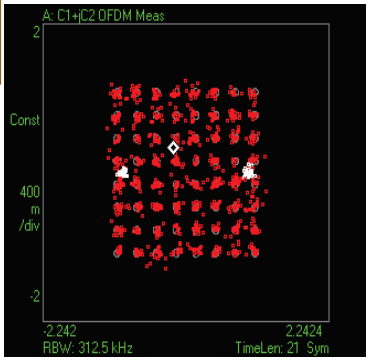
F. Qazi, Q. T. Duong, J. Dabrowski. "Two-Stage Highly Selective Receiver Front-End Based on Impedance Transformation Filtering", IEEE Transactions on Circuits and Systems II, Oct 2014 (Accepted).

Flexible radio sampling receiver front-ends

A 2.4-GHz RF Sampling Receiver Front-End in 0.18-µm CMOS

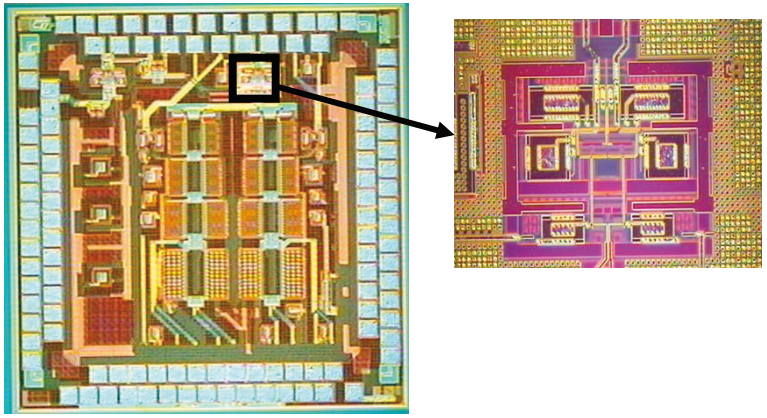






Constellation diagram for a 64 QAM modulated WLAN signal. EVM = 7% RMS (54 Mb/sec)

A 1.4V, 25mW inductor-less wideband LNA in 0.13µm CMOS



Technology	0.13um CMOS
Voltage Gain	17 dB
Frequency range	1-7 GHz
NF	2.4 dB at 3 GHz
IIP3	-4.1 dBm
1dB CP	-20 dBm
Power, at 1.4V	25 mW
Active Area	0.019 mm^2

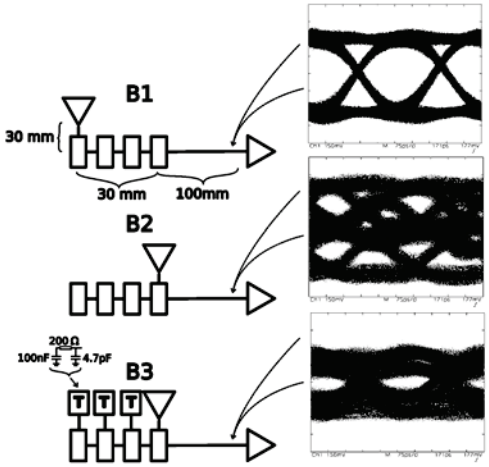
One of the first reported flexible radio sampling receiver front-end for software defined radio

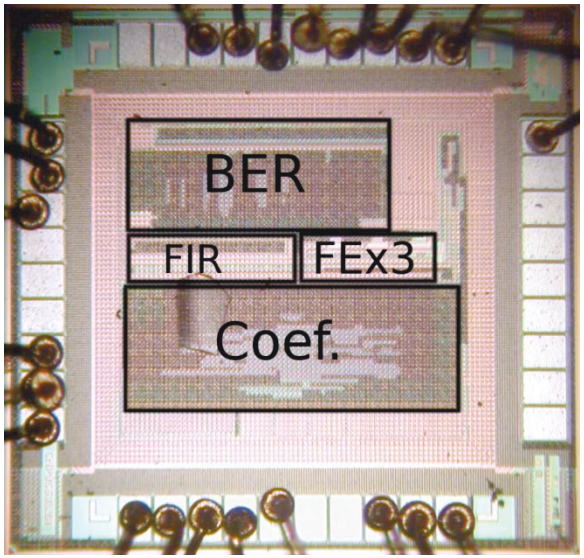
D Jakonis, K Folkesson, J Dabrowski, P Eriksson and C Svensson, "A 2.4-GHz RF Sampling Receiver Front-End in 0.18-µm CMOS". In *IEEE Journal of Solid-Stated Circuits*, Vol 40, No 6, June 2005, pp 1265-1277.

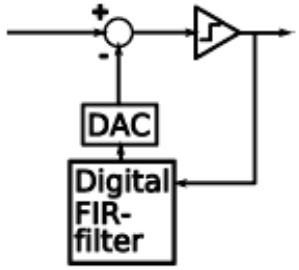
R. Ramzan, S. Andersson, J. Dabrowski, and C. Svensson, "A 1.4V 25mW inductorless wideband LNA in 0.13 mm CMOS", in IEEE International Solid State Circuits Conference (ISSCC'07), pp. 12-13, USA, 2007

Example of earlier work on high-speed digital building blocks, memories, on/off-chip communication/synchronization and clock generators

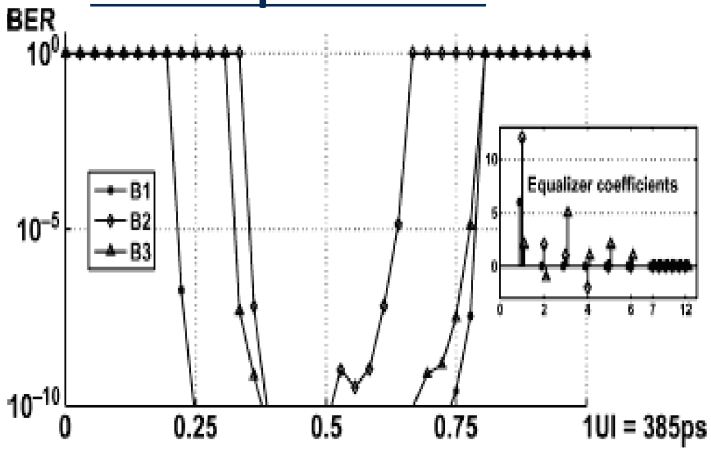
2.6 Gb/s, 93mA, 12 tap 8 bit equalizer receiver for multi-drop DRAM memory bus







After Equalization

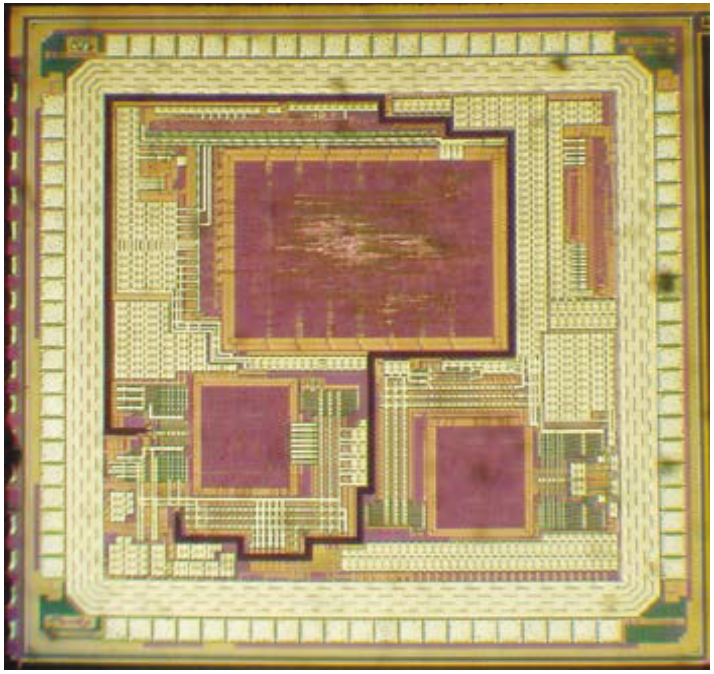


Total equalizer area: 0.187 mm^2

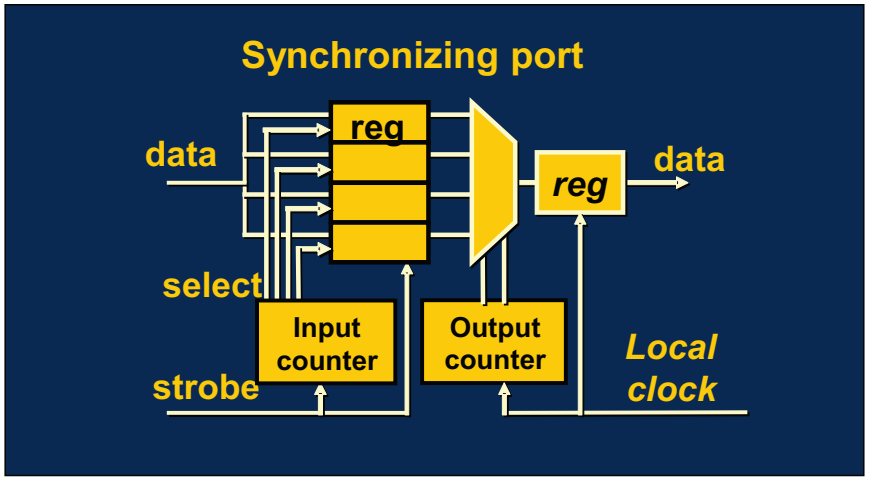
Adaptive 12 tap 8 bit single ended Decision Feedback Equalizer (DFE) receiver and BER measurement circuits in 130nm CMOS, 1.2V.

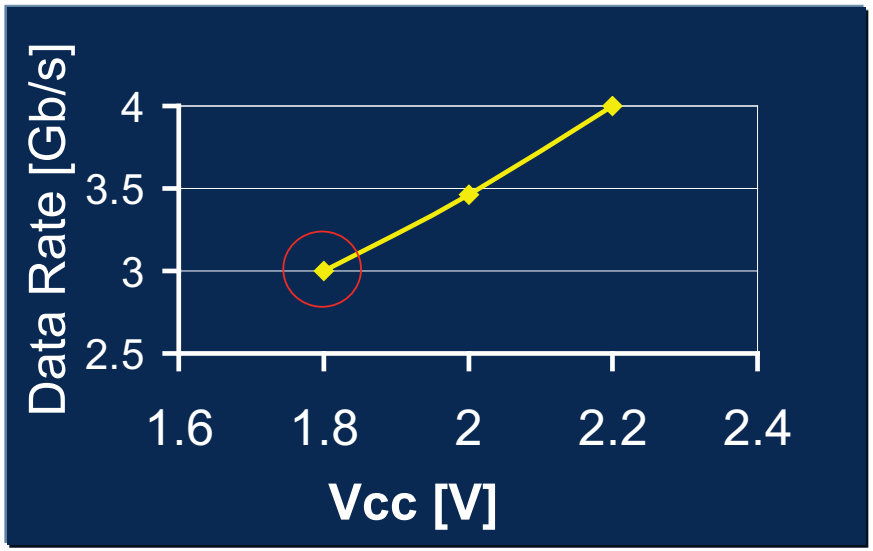
H. Fredriksson and C. Svensson, "Improvement Potential end Equalization Example for Multidrop DRAM Memory Buses", in IEEE Trans. Advanced Packaging, Vol.32, Issue 3, pp: 675-682, August 2009.

Synchronous latency insensitive on-chip communication



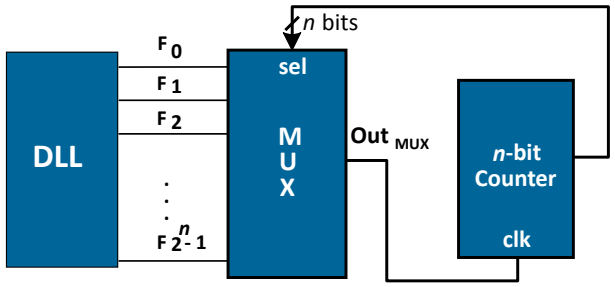
0.18µm CMOS



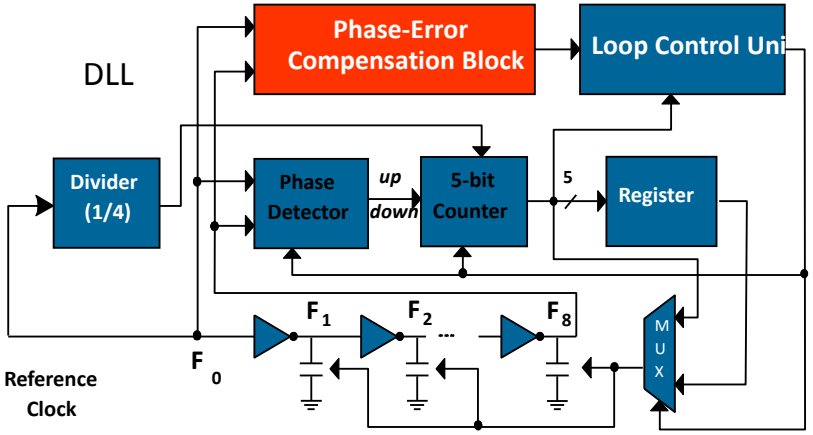


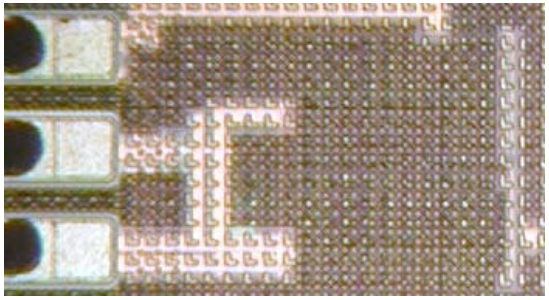
P. Caputa and C. Svensson: "An on-chip delay- and skew-insensitive multi-cycle communication scheme", in *IEEE International Solid-State Circuits Conference (ISSCC' 06)*, pp.444-445, USA, Feb. 2006

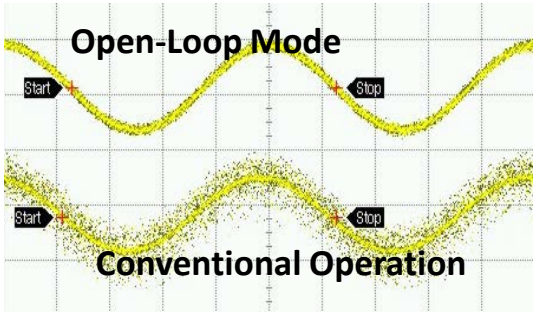
A 2GHz 7mW digital DLL-based frequency multiplier in 90nm CMOS

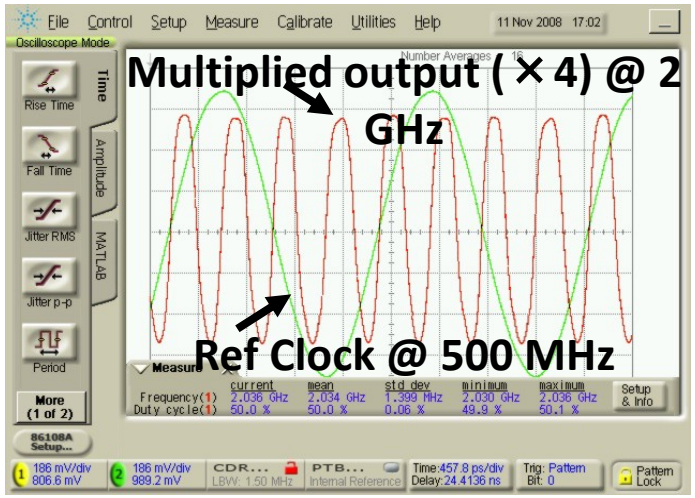


If the number of delay elements in VCDL is *m* then: $f_{LSB} = \frac{m}{2} f_{ref}$









Process: 90-nm CMOS

Area: 0.037 mm^2

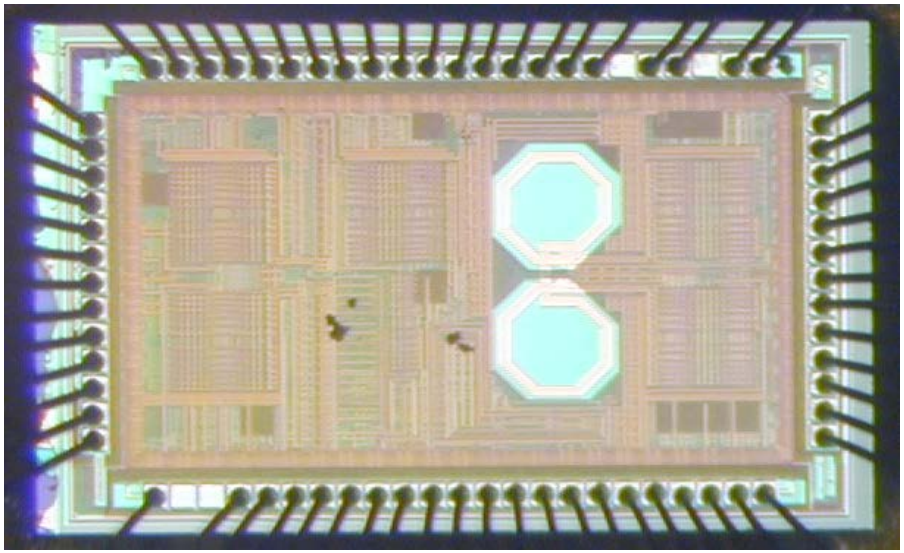
Power: 7 mW at 2 GHz
(6.75 mW DLL, and 0.25 mW FM)

Jitter: rms =1.6 ps, and p-p=9.5 ps

14% power reduction compared to previously reported works.

B. Mesgarzadeh and A. Alvandpour, "A Low-Power Digital DLL-Based Clock Generator in Open-Loop Mode", in IEEE Journal of Solid-State Circuits, vol. 44, no. 7, pp. 1907-1913, 2009.

First reported ‘buffer-less’ resonant clock distribution, with up to 70% power saving

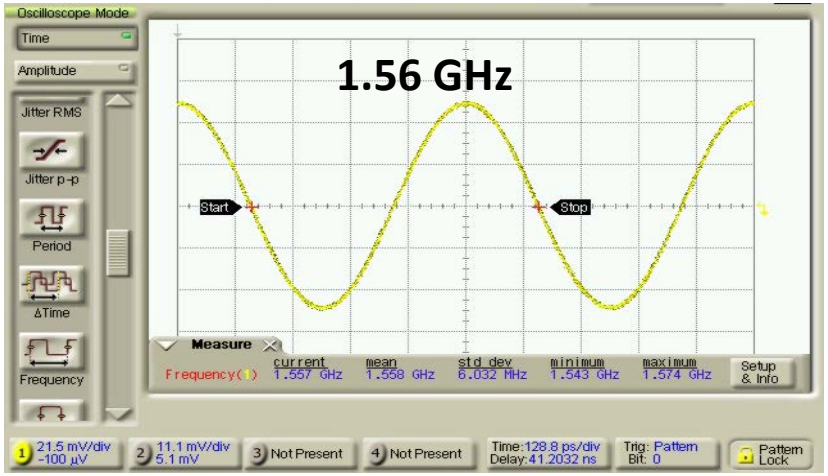


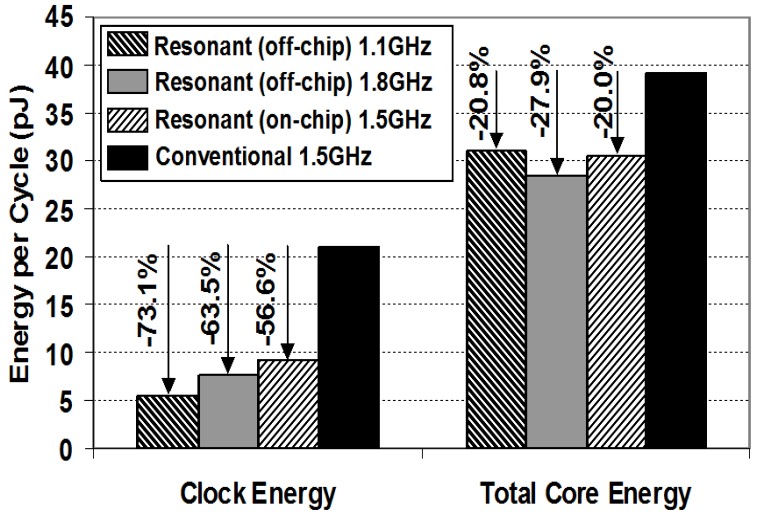
Process: 130nm CMOS
Area: 1.48 X 2.18mm

Clock Frequency: up to 1.8 GHz

29ps p-p jitter at 1.56 GHz

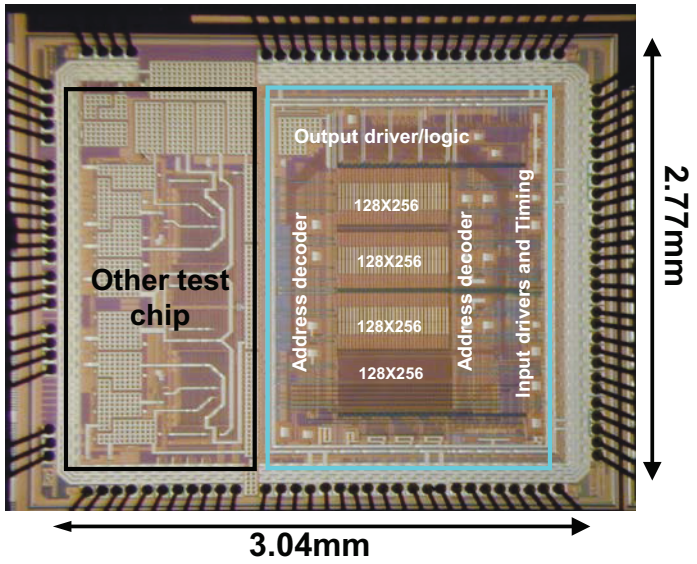
57%-73% lower clock power

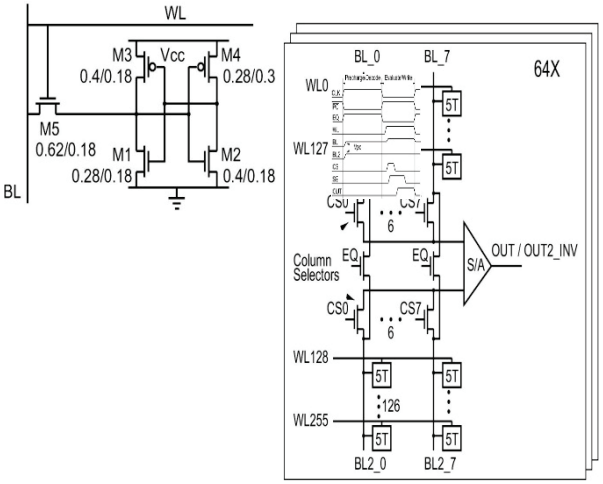


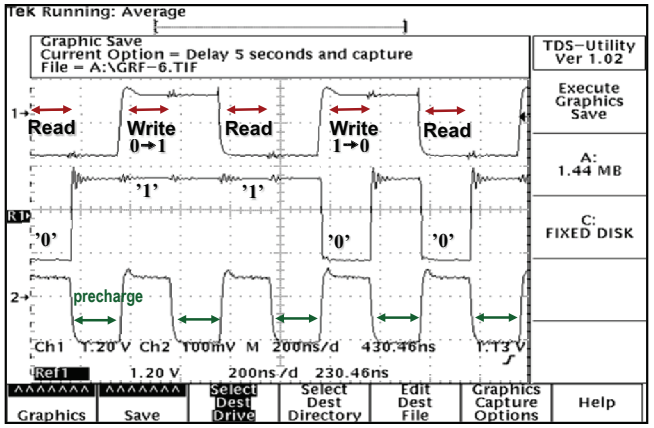


B. Mesgarzadeh, M. Hansson, and A. Alvandpour, “Jitter characteristic in charge recovery resonant clock distribution”, in IEEE Journal of Solid-State Circuits, pp. 1618-1625, July 2007

A high density, low leakage, 5T SRAM for embedded caches







Process: 0.18µm CMOS
Cell area (with logic design rule): 6.30µm^2 (7.99µm^2 for 6T)
Memory area: 0.88mm^2

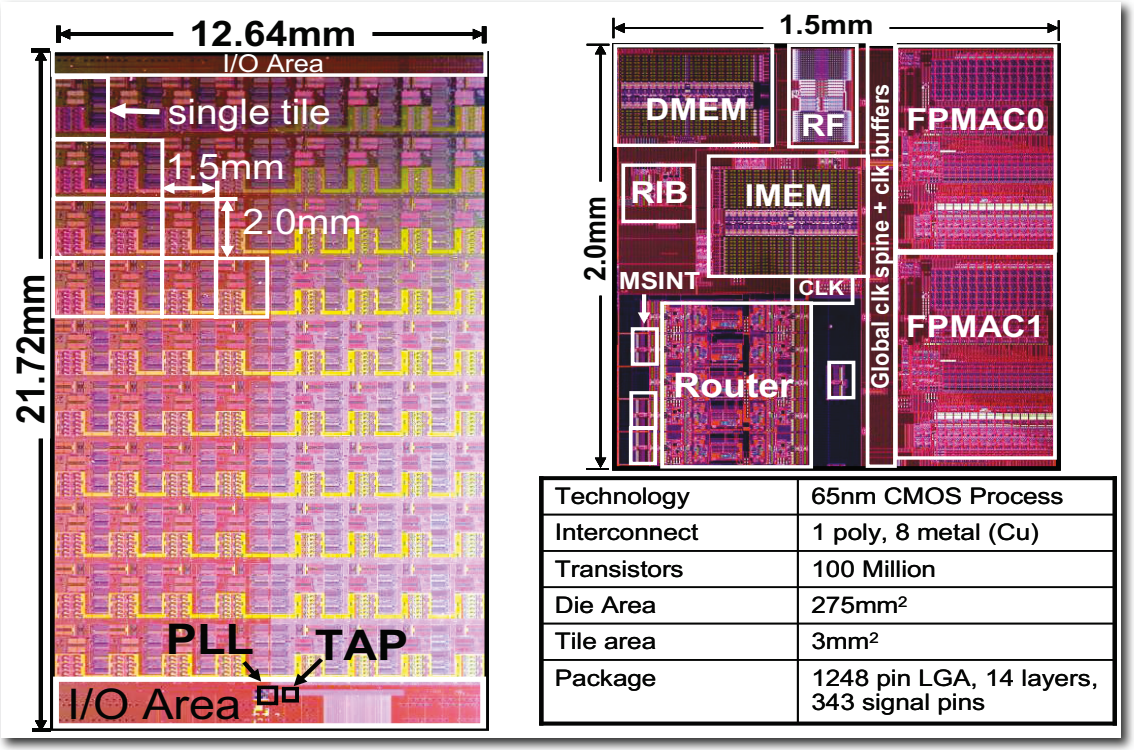
Comparison to conventional 6T cell SRAM:
40% lower cell leakage
70% smaller bitline leakage
22% smaller area
Comparable read/write performance

Full read/write functionality for all 128K 5T-cells
Total read delay of 360ps.

I. Carlson, S. Andersson, S. Natarajan, A. Alvandpour, "A high density, low leakage, 5T SRAM for embedded caches", in European Solid-State Circuits Conference, ESSCIRC, pp. 215-222, Sept 21-23 2004.

Also in Intl. Conference on Memory Technology and Design (ICMTD 07), pp. 185-188, Giens, France, 2007

Contributions to Intel 80 core teraflop processor



Technology	65nm CMOS Process
Interconnect	1 poly, 8 metal (Cu)
Transistors	100 Million
Die Area	275mm^2
Tile area	3mm^2
Package	1248 pin LGA, 14 layers, 343 signal pins

- Sustained 1.01 Teraflops at 97 watts (65nm CMOS)
- Measured power efficiency of 19.4 GFLOPS/Watt

S. Vangal, A. Singh, J. Howard, S. Dighe, N. Borkar, and A. Alvandpour, "A 5.1 GHz 0.34 mm^2 Router for Network-on-Chip Applications", 2007 Symposium on VLSI Circuits, pp. 42-43, Kyoto, Japan, 2007

S. Vangal, Y. Hoskote, N. Borkar and A. Alvandpour, "A 6.2-GFlops floating-point multiply-accumulator with conditional normalization", in IEEE Journal of Solid-State Circuits, vol. 41, pp. 2314-2323, Oct. 2006

S. Vangal, et al, "An 80-Tile 1.28TFLOPS Network-on-Chip in 65nm CMOS", in proceedings of IEEE International Solid State Circuits Conference (ISSCC'07), pp. 98-99, San Fransisco, USA, 2007

Teraflop 80-Core Programmable Processor

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FÖRST OCH FRÄMST MED TEKNIK OCH IT

För racingfantaster
Kör rally i vardagsrummet

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PUBLICERAD 070313, 16:46

Intels nya superchip föddes i Linköping

Processortillverkaren Intel visade för en månad upp sin nya processor Polaris, som ger en vanlig pc superdatorkapacitet. Men grunden till Polaris lades av Linköpingsforskaren Sriram Vangal i hans licentiatavhandling från 2006.

Annons

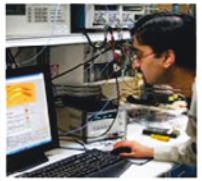
Infranetbranschen söker landets 300 vassaste medarbetare
Eltel säkrar att samhällets livsviktiga el- och telenät alltid fungerar. Vi kallar det Infranet. Nu söker vi beredare, tekniker och ledare mfl. Läs mer om tjänsterna
Vi säkrar samhällets livsviktiga Infranet
ELTEL networks

- De byggstenar som vi designat på LiU bildar grunden för Intels teraflopchip Polaris, säger Sriram Vangal i ett reportage på LiU:s hemsida.

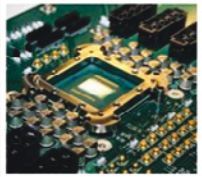
Processorn är uppbyggd kring en krets med 80 processorkärnor, inte större än en fingernagel. Den har kapaciteten drygt 1 teraflop, men förbrukar trots det bara 62 watt. Det är mindre än vad många av dagens pc-processorer med betydligt beskedligare prestanda förbrukar.

Sriram Vangal har delat sin forskartid mellan Intel och LiU.

Arbetet med teraflopprocessorn beskrivs i Sriram Vangals 60-sidiga licentiatavhandling från LiU 2006. Resultatet av hans forskning tillsammans med professor Atila Alvandpour har också publicerats i flera vetenskapliga artiklar, skriver LiU-reportern Åke Hjelm.



LiU-Intel blev en lyckad kombination. Här är Sriram Vangal i labbet.



Det revolutionerande med Polaris är arkitekturen med 80 kommunicerande kärnor, tre kvadratmillimeter stora, tätt

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EE Times: Latest News

Intel's teraflops chip uses mesh architecture to emulate mainframe

CAREER CENTER
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R. Colin Johnson

Page 1 of 2

EE Times
(02/12/2007 9:00 AM EST)

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REPRINTS

PORTLAND, Ore. — Research into competing architectures for the multicore processors of the future will take center stage this week when Intel Corp. demonstrates its Teraflop Research Chip—code-named Polaris—at the International Solid-State Circuits Conference in San Francisco.

Thank you

For further information about our research and education or in case of interest in future collaboration, please don't hesitate to contact us.

Regards

Atila Alvandpour, Professor, Division Head
Email: Atila.Alvandpour@Liu.se